

# Controller IC For NAND Type Flash Memory To 16G Bytes, GBDriver® XR

## Conforming to RoHS Directive

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Introducing the most-advanced product with support for general SRAM bus. In short, it allows easy realization of low-cost home information appliances with only one 8mm-square chip based on a high-capacity NAND type flash memory controller.

One chip can control up to eight (up to 16G bytes) NAND flash memories (64M bit - 16G bit products). It permits simple attainment of low-cost systems based on the next-generation 8G bit and 16G bit high-capacity memory.

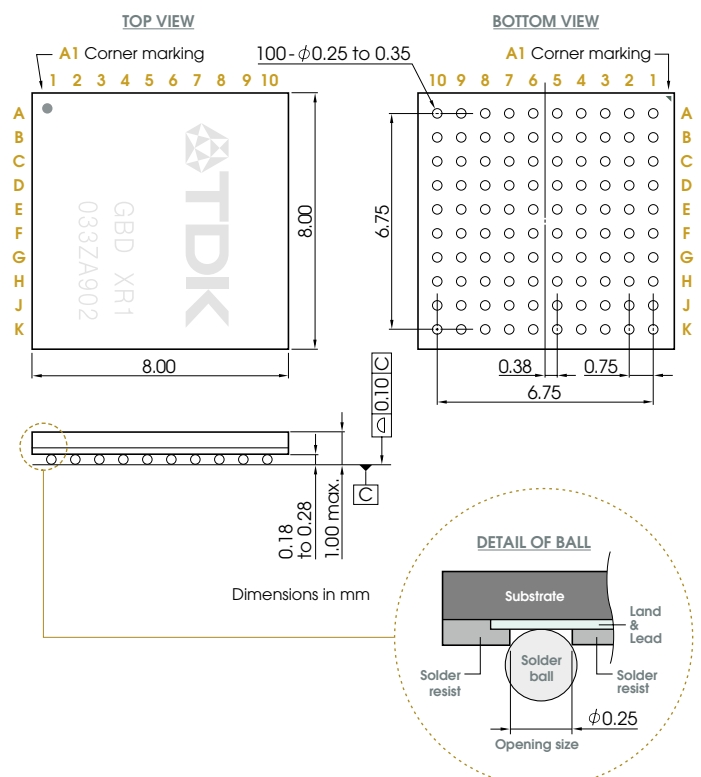
As of January 2005, there are up to 4G bit of NAND flash memory products available. It is anticipated that the makers will launch 8G bit (1G byte) and 16G bit (2G byte) products near the end of 2005 or the beginning of 2006.

It supports – a world first – general-purpose SRAM interfaces, and read/write performance has been further improved. The NAND flash memory can be controlled through a direct connection to the CPU bus, allowing systems without interfaces for hard disks, such as ATA/IDE, to use high-capacity, low-priced NAND flash memories for storing system OS, system work areas, user data, and so forth.

Of course, similar to conventional types, it supplies a unique all-in-one one-chip solution with all control functionality concerning the NAND flash memories. Moreover, using an ultra-small/low-profile 8mm-square VFBGA-100pin package, it can be easily integrated into systems such as handheld information devices, business terminal devices, and small IT home appliances, which are widely expected to be leading forces in the NAND-type flash memory market.



## Shapes and dimensions



## General-purpose SRAM interface

Unlike the interfaces of silicon discs and Compact Flash cards, a general-purpose SRAM interface is used to connect to the host. This allows the use of high-capacity, low-cost NAND flash memories even if inexpensive LSI, which support no IDE channel, are used in the system.

## All-in-one one-chip solution

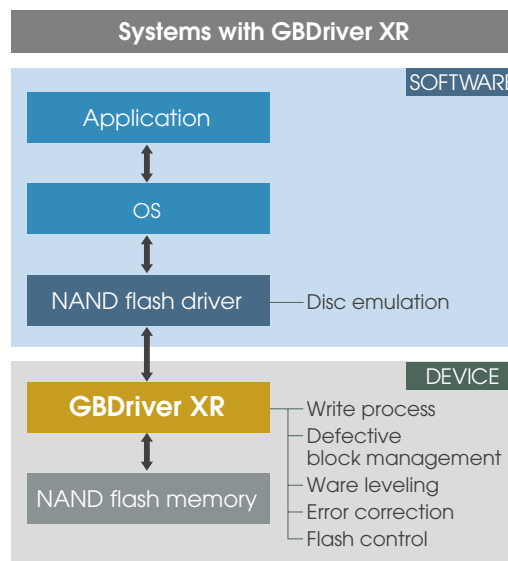
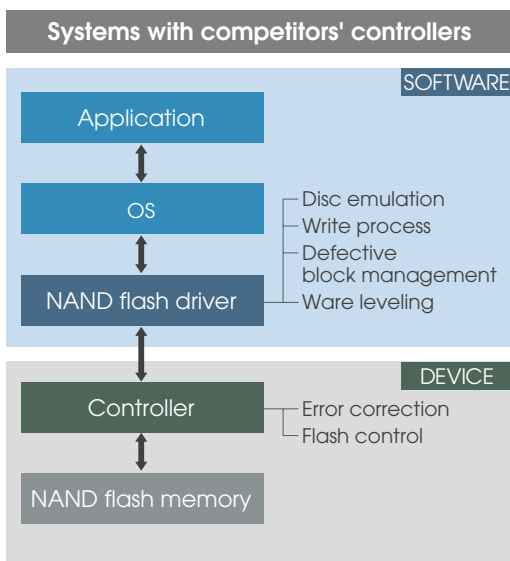
Every control function of NAND flash memories, such as error-correcting circuits, block management, address control, etc., are included, allowing NAND flash memory to be used for system memory storage merely by creating a low-level driver which controls a memory-mapped ATA register. This one chip can solely handle all memory tasks, focusing the efforts of the device design and development workforce on the system evolution of the platforms for rapid facilitation of next-generation device establishment.

# GBDriver® XR



### Basic characteristic/rating

Host interface	120ns (BUS cycle)	
Flash interface	90ns	
Power source specification	Host I/F	2.7 to 3.6V
	Core	2.7 to 3.6V
	Flash I/F	2.7 to 3.6V
System clock	33 MHz	
operating temperature range	-40 to +85 °C	



Our competitors' systems process the management of flash memories (write process, defective block management, ware leveling, and so on) on the software of the host, so wasting the CPU power of the host.

In a system with TDK GBDriver XR, the management of flash memories is performed inside GBDriver XR, allowing flash memories to be accessed without wasting the loss of CPU power. This also allows more reliable systems because there are very few OS-dependent processes. TDK has plans to develop and offer disc emulation drivers for each OS as part of the technical support provided by flash application staff members.

### Reliability in data writing

To countermeasure flash memory's time-lapse degradation, TDK's original, accurate, control methods, which have proven their quality in the GBDriver series, are applied. For improved reliability in data writing for flash memories, features such as the memory control method, which blocks writing to defect cells, are integrated. Also, a function is integrated to dynamically verify the detection of a potentially defective physical block, so realizing the high-reliability required for NAND flash memories in embedded systems.

### Avoiding centralization of writing blocks

For rewriting of FAT, or directory areas, an original method is used so that writing will not be centralized at certain blocks.

### Avoiding writing to blocks that were not completely erased

Writing to flash memories is performed only in "the blocks where all memory cells are completely erased", avoiding writing in "the blocks with the possibility of read error" due to power failures at the moment of writing, or erasing processes, and to "the blocks where one or more memory cell(s) has had an incomplete erasure" due to time-lapse degradation of flash memory cells.

### Quick Read/Write

The same flash control architecture as that of the controller for TDK CompactFlash cards and silicon disc modules, such as GBDriver RA Series, is used. Plus, being directly connected to the system bus makes it fast, achieving 6M byte/second (equivalent to 40 times faster\*) through a burst write. This contributes to reducing kernel load times of diverse systems (The burst read speed is also 20% faster than that of our current products).

\*Equivalent value where 150K byte/second is considered the one-fold speed

## GBDriver® XR



### Error correction/restoration

For bit-error occurrence during the read, which must be considered in system design for embedding purposes, a feature is integrated to correct such errors upon detection of correctable bit-error and to transfer the data in those blocks to safe ones. This provides adequate reliability for OS storing areas of embedded devices where the read occurs frequently.

### Avoidance of the write through detection and verification of unstable blocks and restoring reversible defective blocks

A feature is included to detect and check unstable blocks of flash memories. As a result, writing to the blocks with a risk of reading error is avoided, and reversible defective blocks are saved. This is a TDK original memory management/control technology, preventing unreadable incidents due to the write to incompletely erased blocks, and averting reduction of memory capacity due to increased correctable defective cells.

### Detailed verification by the "Write & Verify" command ensures further reliability advances

The "Write & Verify" command, which verifies existence of the read error at each write to every sector, is supported. GBDriver only writes to completely erased blocks, and with the "Write & Verify" command being used together when writing system data such as that of OS, a higher level of reliability is ensured.

## Examples of applied devices/systems

Although NAND flash memories were originally designed for the file systems and memory cards of consumers, their application in recent years has extended to storing system OS, user data, and system data, accompanied by the rapidly improved functionality and significant spread of the use of small information devices, digital AV systems, IT home appliances, car-navigation systems, ITS, business terminal devices, and so forth.

TDK's GBDriver Series, with its original architecture providing the most advanced product in the industry, has received high recognition and been widely used both in consumer and embedded uses as an innovative device with all functions required for the outstandingly reliable employment of NAND flash memory integrated into one chip.

## GBDriver® XR



Mobile phone/PDA/Electronic organizer/Printer/Scanner/Projector/HDD/DVD drive/CD-R/RW drive  
CD-ROM drive/Broadband router/Access point/Network storage/Multimedia device/Digital camera  
Digital video camera/Digital audio system/Memory audio player/Portable DVD player/IT home appliance  
Home theater system/Set-top box/Plasma TV/Wide liquid crystal TV/DVD/HDD recorder  
Car-navigation system/GPS system/ITS/Monitoring system for surveillance/Diverse security systems  
Handy terminal for business use/POS register/FA control device/Industrial robot/Measuring device/ME device

## Information on related products

# Controller IC For NAND Type Flash Memory To 8G Bytes, GBDriver® RA4

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**GBDriver supports "CF+ and CompactFlash Specification Version 2.1" (maximum transmission speed: 16.6M byte), the latest CompactFlash standard.**

**Offering an actual transfer rate that's more than 1.8 times faster when reading and about 1.4 times faster when writing**

- Supporting PIO-Mode4 with a maximum transfer rate of 16.6M byte/s, much faster than that of the conventional host interface (PIO-mode2), which was the bottleneck in attaining the potential of accelerated NAND flash memories. Compared to the conventional RA3 which supports PIO-Mode2, a read performance that's more than 1.8 times faster and a write performance that's about 1.4 times faster can be achieved.
- With embedded systems, such as operating systems and data systems, the bootup time or loading time of the kernels or application programs can be greatly reduced. Also, for devices where capability is determined directly by the speed of data transfer, such as high-resolution single-lens reflex digital cameras, for which faster activation and continuous shooting are required, performance that overcomes conventional limitations is offered.
- One chip can control up to four (up to 8G bytes) NAND flash memories (1Gbit - 16G bit products), allowing easy realization of rapid high-capacity systems at low cost, based on the next-generation 8G bit (1G bytes) and 16G bit (2G bytes) memory chips.

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